REMARKS

The Office Action dated January 14, 2005 (Paper No. 011105) has been received and the Examiner's comments carefully reviewed. Prior to entry of this paper, Claims 1-20 were pending. Claims 1-5 and 8-20 were rejected, and Claims 6 and 7 were identified as being allowable if re-written in independent form. In this paper, Claims 1, 2, 6, 9, 10, 13, 17, and 20 are amended. Claims 1-20 are currently pending. No new subject matter has been added. For at least the following reasons, Applicants respectfully submit that each of the presently pending claims is in condition for allowance.

Claims 6 and 7--Allowable Subject Matter

Claims 6-7 were objected to, but were identified as being allowable if re-written in independent form. In this paper, Claim 6 is re-written in independent form, and Claim 7 retains its dependency to Claim 6.

Claims 1, 3-5, 8-10, and 17-19

Claims 1-5 and 8-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Nebel (U.S. PAT. 6,392,440).

It is respectfully submitted that the rejection to Claim 1 is moot in light of the amendment to Claim 1. Further, it is respectfully submitted that Claim 1 as amended is allowable at least because Nebel does not disclose "a second shunt circuit that is coupled between the second bias node and the low-range node, wherein the second shunt circuit includes a switch circuit that is arranged to close if a voltage associated with the full-range node corresponds to a logic high", as recited in Applicant's Claim 1 as amended.

Nebel describes an inverter 1, which includes diodes MN11 and MP11 as shown in Fig. 1 of Nebel. The remainder of this paragraph (in this paper) continues to refer to inverter 1 of Nebel as shown as Fig. 1 of Nebel and described in Col. 4, line 11 through Col. 5, lines 37 of Nebel. Terminal 5 is held at 1.4V, and terminal 6 is held at 3.6V. When inverter input signal IN is at 5V, switching transistor MN21 is turned on, and switching transistor MP21 is turned off. Also, when

inverter input signal IN is at 5V, transistor MP11 prevents the potential at node N1 from exceeding approximately 3.6V by discharging leakage current from transistor MN11 if the voltage at node N1 exceeds approximately 3.6V. When inverter input signal IN is at 0V, switching transistor MN21 is turned off, and switching transistor MP21 is turned on. Also, when inverter input signal IN is at 0V, transistor MN22 prevents the voltage at node DN from exceeding approximately 3.6V. Also, when inverter input signal IN is at 0V, diode MP11 is "back-biased", and node N1 is floating.

In contrast, Applicant's Claim 1 as amended recites, "a second shunt circuit that is coupled between the second bias node and the low-range node, wherein the second shunt circuit includes a switch circuit that is arranged to close if a voltage associated with the full-range node corresponds to a logic high." Transistor MP11 of Nebel is a diode that is coupled between terminal 6 and node N1. However, transistor MP11 of Nebel is not "closed" when inverter input signal IN corresponds to a logic high. Rather, in Nebel, when inverter input signal IN corresponds to a logic high, diode MP11 is "back-biased", and node N1 is floating.

For at least these reasons, Claim 1 is respectfully submitted to be allowable, and notice to that effect is respectfully requested.

Claim 17 is respectfully submitted to be allowable for reasons similar to those stated with regard to Claim 1.

Claims 3-5 and 8 are respectfully submitted to be allowable at least because they depend on Claim 1, which is proposed to be allowable. Claim 18 and 19 are respectfully submitted to be allowable because they depend on Claim 17, which is proposed to be allowable.

The rejections to Claims 9 and 10 are respectfully submitted to be moot in light of the amendment to Claims 9 and 10, respectively.

Claim 9 is respectfully submitted to be allowable at least because Nebel does not disclose "first shunt circuit is configured to isolate the first bias node from the high-range node if the full-range signal corresponds to a logic high", as recited in Applicant's Claim 9 as amended.

Claim 10 is respectfully submitted to be allowable at least because Nebel does not disclose "first shunt circuit is configured to short the first bias node to the high-range node if the full-range signal corresponds to a logic low", as recited in Applicant's Claim 10 as amended.

Claim 2

The rejection to Claim 2 is respectfully traversed. Claim 2 was re-written in independent form, and further amended for increased clarity.

It is respectfully submitted that Claim 2 is allowable at least because Nebel does not disclose "the first bias node and the second bias node have approximately the same voltage", as recited in Applicant's Claim 2 as amended.

In Nebel, terminal 5 (LOW) has a voltage of 1.4V, and terminal 6 (HIGH) has a voltage of 3.6V. See column 4, lines 37-39 of Nebel. Also Nebel operates with 5V signals and can be manufactured using 3.3V technology. Accordingly, terminal 5 is not approximately the same voltage as terminal 6.

A difference of 2.2 volts may result in "approximately the same voltage" at a much higher supply voltage, e.g. 16V. For example, in one embodiment of Applicant's invention, signal F_RANGE may swing from 0V to 16V, voltage VSN may be 9.1 V, and voltage VSP may be 6.9V. In this embodiment, since VSP and VSN are both approximately mid-supply (8.0V), VSP and VSN are approximately the same voltage.

In contrast, in Nebel, terminal 5 is 1.4V, which corresponds to a logic low in the circuit, and terminal 6 is 3.6V, which corresponds to a logic high in the circuit. Accordingly, in Nebel, terminal 5 is not approximately the same voltage as terminal 6.

Claims 13-16 and 20

The rejections to Claims 13-16 and 20 are respectfully traversed. Claims 13 and 20 were amended for increased clarity.

Claim 13 is respectfully submitted to be allowable at least because Nebel does not disclose "ensuring that at least one of: the low-range node is driven during a full cycle of the full-range

signal, and the high-range node is driven during the full cycle of the full-range signal", as recited in Applicant's Claim 13.

As previously discussed, in inverter 1 in Nebel, when inverter input signal IN corresponds to a logic high, diode MP11 is "back-biased", and node N1 is floating. Accordingly, inverter 1 in Nebel does NOT drive the low-range node during the full cycle of the full-range signal.

Also, in Nebel, when inverter input signal IN corresponds to a logic low, diode MN11 is "back-biased", and node P1 is floating. Accordingly, inverter 1 in Nebel does NOT drive the high-range node during the full-cycle of the full-range signal.

Claim 20 is respectfully submitted to be allowable for reasons similar to those stated with regard to Claim 13.

Claims 14-16 are submitted to be allowable at least because they depend on Claim 13, which is proposed to be allowable.

Conclusion

It is respectfully submitted that each of the presently pending claims (Claims 1-20) are in condition for allowance and notification to that effect is requested. The Examiner is invited to contact Applicant's representative at the below-listed telephone number if it is believed that prosecution of this application may be assisted thereby. Although certain arguments regarding patentability are set forth herein, there may be other arguments and reasons why the claimed invention is patentably distinct. Applicant reserves the right to raise these arguments in the future.

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Respectfully submitted,

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